REMARKS/ARGUMENTS

In the Office action dated November 23, 2005, the Examiner continued a provisional double patenting rejection. Claims 1-6 and 9-14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U. S. Patent No. 6,825,519 B2 to Li *et al.* in combination with U. S. Patent No. 6,407,422 B1 to Asano *et al.* Claims 7, 8, 15 and 16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over '519 in combination with '422 and further in combination with U. S. Patent No. 6,664,116 B2 to Li *et al.* Claims 17 - 20 were not specifically rejected under any of the usual statutory provisions of 35 U.S.C.

In the Specification, no changes

In the Claims, claim 8 is amended.

The Invention

The invention is a method of forming an indium-containing thin film on a silicon substrate, patterning the indium-containing thin film and depositing a layer of ferroelectric material on the indium-containing thin film in a process which eliminates the need for subsequent patterning of the ferroelectric layer. The use of the indium-containing thin film as a bottom electrode for a ferroelectric stack allows for much faster deposition of the ferroelectric material on the indium-containing thin film than on the surrounding material, thus simultaneously depositing and patterning the ferroelectric. See page 7, table 3 of the Specification.

The Applied Art

The Examiner has applied two patents by Li *et al.*, which include all of the inventors hereof. U. S. Patent No. 6,825,519 B2 describes selective deposition of a PGO thin

film, but, as the Examiner correctly points out, does not teach use of an indium-containing bottom electrode. '519 and U. S. Patent No. 6,664,116 B2 describe use of a ferroelectric seed layer.

The Examiner has applied new art in the form of U. S. Patent No. 6,407,422 B1, granted June 18, 2002, to Asano *et al.*, as demonstrating provision of an indium/indium oxide bottom electrode. It is noted that this reference issued well before the filing of the instant application and could have easily been applied in response to the initial filing. Asano *et al.* describe fabrication of a semiconductor capacitor, which may include a metal suboxide layer 51 and a diffusion barrier 52. In the patentee's recitation of virtually the entire periodic table in col. 5, lines 45-57, indium is identified as a possible component of the metal sub-oxide in layer 51. In the description of barrier layer 52, indium is not mentioned. Film 51 is formed partially on a silicide layer 53 and partially on an insulating layer 13. A layer of dielectric 33, which may be a perovskite material, is formed on barrier layer 52. Thus, the structure of '422 is:

perovskite
barrier layer - not containing indium
metal sub-oxide, which may contain indium
substrate

The Claims

The claims, as amended in response to the previous Office action remain unchanged. Claim 1, as previously presented, requires:

ferroelectric - which may be perovskite
indium containing thin film
substrate

Thus, there is an additional layer in the applied art, which does not contain indium, and which is in contact with the ferroelectric layer. It is clear that to omit the barrier layer from '422 would

render the device inoperative.

While Applicants acknowledge that Asano *et al.* identify indium oxide as one of the possible 35 metal suboxides which may be used as layer 51, col. 5, lines 45-68, when it comes to the preferred embodiment of layer 51, indium is nowhere mentioned: not in the Specification, as in col. 6, lines 1-19, describing the preferred embodiment, nor in the description of prior art (Fig. 5, col. 2, lines 1-54), nor in the claims, wherein the bottom electrode is recited as containing the metal suboxide layer and the barrier layer. At many locations in the '422 specification, the components of the metal suboxide layer are discussed. The one and only mention of "indium" is in the laundry list of 35 elements. See claims 10 and 11, wherein the metal suboxide layer is recited as containing many metal elements, but wherein indium is *NOT* one of the recited elements. Thus, it appears clear that the patentees of '422 recognized that their semiconductor device was not suitable for use of an indium or indium oxide bottom electrode.

Claim 1 is clearly allowable over the applied art.

Further, claims 2-3 require forming an oxide layer and high-k oxide layer, respectively on the substrate, which occurs before deposition of the indium-containing thin film. The Examiner's combination still does not render these steps obvious, as the combination of '519 and '422 still does not provide and oxide layer between the substrate and an indium-containing layer, and does not eliminate the barrier layer of '422. The Examiner's combination has an indium-containing layer on the substrate and a barrier layer on the indium-containing layer. The claims do not read on this structure or method. Claims 2 and 3 are allowable over the applied art.

With respect to claim 4, while '422 undoubtedly requires patterning the indium-

containing metal-suboxide layer, if present, it does not have the layers in the order required by Applicants. Claim 4 is therefore allowable over the applied art, or allowable with its allowable parent claim.

Claims 5 - 8 are allowable with their allowable parent claims. Claim 8 is amended to correct dependency.

Claim 9 specifically requires that the layer ordering is: silicon substrate - indium oxide thin film - PGO layer. Again, '422 and '519 do not teach these steps: there is no way that the indium oxide layer is the bottom electrode in the '422/'519 Examiner's combination, as there is a barrier layer 52, which does not contain indium, in contact with the ferroelectric layer. There is no teaching which allows removal of '422 barrier layer 52 to form the method of claim 9. Claim 9 is clearly allowable over the applied art because the applied art requires deposition of a layer which is not required by the claims nor present in the device constructed according to Applicants' method of the invention.

Claim 10, 11 and 12 are allowable for the reasons set forth in connection with claims 2, 3 and 4, respectively.

Claims 13-16 are allowable with their allowable parent claims.

Claims 17 to 20 are not specifically rejected under any of 35 U.S.C. § 112, 35 U.S.C. § 103(a), or 35 U.S. C. § 102. These claims are allowable for the reasons set forth in connection with claim 1 and 9, in that the applied and cited art does not teach not suggest the steps of Applicants' method of the invention. Further, the structure created by the Examiner proposed combination of '422, 519 and '166 does not produce a structure consisting of a

substrate - a silicon oxide layer - an indium oxide layer - and a ferroelectric layer. The Examiner's combination, at best is substrate - metal suboxide, which may contain indium - non-indium containing barrier layer - ferroelectric layer. The claims are quite specific as to the ordering and content of the layers. No other layers may be deposited, and no layers may be omitted. As to the Examiner's question regarding the thickness of the ferroelectric layer on the indium oxide, this element is clearly recited in the Specification, Table 3. The claim, as presented, recites the advantage of the deposition in that the PGO layer need not be etched to remove PGO from the surrounding silicon oxide layer, as the deposition rate of PGO on indium oxide is much greater than the growth rate of PGO in silicon oxide. Contrary to the Examiner's assertion that the applied art teaches Applicants' structure, Applicants have repeatedly pointed out in this correspondence that the applied art does not teach the structure, and does not teach the elements of claim 17, which, because the elements thereof are neither taught nor anticipated, is clearly allowable over the applied art. Claim 17 is further allowable for the reasons set forth in connection with claims 1 and 9.

Claims 18-20 are allowable with their allowable parent claim.

The invention and the claimed subject matter are commonly owned during all relevant times.

In light of the foregoing amendment and remarks, the Examiner is respectfully requested to reconsider the rejections and objections state in the Office action, and pass the application to allowance. If the Examiner has any questions regarding the amendment or remarks, the Examiner is invited to contact the undersigned.

Request for Extension of time in Which to Respond

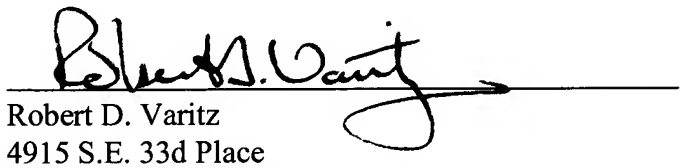
Applicants hereby request a one-month extension of time under 37 C.F.R. § 1.136. The attached PTOForm 2038 Credit Card authorization for $910.00 includes the amounts of $790.00 for the RCE filing fee and an amount of $120.00 for the one-month extension fee. The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any over-payment to Account No. 22-0258.

Customer Number

55376

Respectfully Submitted,

ROBERT D. VARITZ, P.C.



Registration No: 31436
Telephone: 503-720-1983
Facsimile: 503-233-7730

Robert D. Varitz
4915 S.E. 33d Place
Portland, Oregon 97202